REMARKS

Claim 5 is amended, no claims are canceled, and no claims are added; as a result, claims 1-24 are now pending in this application.

Claim 5 is amended to clarify the claim. The amendment to claim 5 is not a narrowing amendment.

§112 Rejection of the Claims

Claim 5 was rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectfully submits that the claim amendment contained herein provides independent claim 5 with proper antecedent basis and requests that this rejection be withdrawn. Applicant thanks the Examiner for pointing out the inadvertent typographical error.

§103 Rejection of the Claims

Claims 1-24 were rejected under 35 USC § 103(a) as being unpatentable over Shibata et al. (U.S. Patent No. 5,754,838) in view of IBM "16mb Double Data Rate Synchronous Graphics RAM". Applicant respectfully traverses this rejection.

The cited reference of Shibata is seen as teaching a synchronous DRAM (SDRAM) that generates an internal clock signal that is different from the external clock signal. See column 3, lines 3 to 7 stating that unlike a conventional synchronous DRAM, the external clock signals CLK are not used as they are, but instead the internal clock signals are generated by a PLL circuit included in the clock input buffer 1. The device of Shibata is a synchronous DRAM as stated at least at column 1, line 9; column 2, line 61; column 3, line 3; and from figure 3 and the discussion relating to figure 3 at column 7, line 38. Applicant respectfully disagrees with the Examiner's statement on page 2 of the Office Action that the cited reference teaches halting the operation of the PLL and using the external clock as the internal clock. The section of the cited reference indicated by the Examiner is seen as teaching the use of a PLL in the case of "extremely slow clock signals" (see column 14, line 67) for inspecting the devices using a test mode for "developing and designing devices" (see column 15, lines 1-2). Thus the cited

reference is not seen as teaching the use or operation of a SDRAM without synchronizing the internal clock to the external clock, but merely a test method. Thus the cited reference is not seen as having any teaching with respect to an arrangement of a first mode of operation not using a lock loop circuit, and a second mode of operation using a lock loop circuit, as recited in the pending claims presented herein.

The cited reference of Shibata is seen as teaching a SDRAM having selectable programmable delays such as shown in figure 7 and discussed at least starting at column 10, line 10 of the specification. The simple voltage controlled oscillator discussed starting at column 7, line 38 is said to be non stable if the difference between the internal clock signal clk is too large as compared to the external clock signal CLK. The cited reference teaches that a SDRAM can be made that can operate in a stable fashion with different external clock frequency ranges, such as 200-300MHz wherein it is taught that input A8 is high and input A9 is low in figure 7, thus activating tristate inverter 3 and enabling the synchronization to occur with the shortest of the three taught ring oscillator delay lines comprising inverters 1 and 2. The cited reference teaches that external clock signals having a range of from 100-200 MHz will have input A8 at a low state and input A9 at a high state, thus activating the tristate inverter 8 and enabling the intermediate ring oscillator delay line. For external clock signals having a range of from 50-100 MHz both input A8 and input A9 are at the low state, thus activating the tristate inverter 17 and enabling the longest ring oscillator delay line. Applicant respectfully submits that a reference teaching variable delay lines for synchronizing an internal clock signal clk to various different ranges of external clock signals CLK is an inappropriate reference to apply to a claimed invention including a mode having no DLL and a mode having a DLL. This is so at least because the cited reference never operates with out the internal clock being synchronized with the external clock, even in the test and design phase where it is stated to be possible to use the external clock directly in extremely low clock rate conditions. Applicant submits that a reference that is always operating in a DLL mode is an inappropriate reference for any suggested combination of references to be used against a claimed invention having a first mode of operation not using a lock loop circuit, and a second mode of operation using a lock loop circuit, as recited in the claimed invention, and that forbidden hindsight has been used to make the suggested combination of references.

The cited reference of IBM, which is cited by applicant and incorporated by reference on page 3 of applicant's specification, is seen as teaching one of two known modes of operation of a dual data rate SGRAM as discussed in applicant's specification at least at page 7, second paragraph where the first mode is a non-DLL mode and the second mode is the IBM mode of using the DLL at all operations. Applicant respectfully disagrees with the Examiner's statement on page 3 of the Office Action that the IBM reference teaches operating modes using the mode register, and submits that the mode register may be seen on page 4 to control the latency period and the length of the read burst, and on page 6 the mode register is stated to set the CAS latency, the addressing mode, burst length, DLL reset and test mode. No where can applicant find any support for the contention that the cited IBM reference describes or suggests an arrangement that does not use the DLL in any memory operating mode. The cited portion of the reference indicated by the Examiner as teaching internally disabling the DLL, is seen as referring only to the memory refresh mode, which is not an operational mode, where the DLL is disabled and the clock is ignored (clearly not an operational mode) "to reduce power". The other described mode is the power down mode (clearly not an operational mode) "to reduce power consumption". Applicant respectfully submits that the cited IBM reference does not describe or suggest an arrangement that has "*a logic circuitry coupled to the memory array configurable to operate the single memory device in a first mode having delayed lock loop (DLL) capability and in a second mode having non-DLL capability*" as recited in independent claim 1, and similarly in the other pending claims. A power down mode is not operating a memory device, nor is a test mode or a refresh mode.

Applicant respectfully submits that the suggested combination of references fails at least because neither reference describes or suggests an arrangement having the features of a "*memory array configurable to operate the single memory device in a first mode having delayed lock loop (DLL) capability and in a second mode having non-DLL capability*" as recited in independent claims 1 and 5. Applicant respectfully submits that the suggested combination of references fails at least because neither reference describes or suggests an arrangement having the ability to "*operate in a first mode and a second mode, the first mode and the second mode each relating to a different alignment of output data as to a read line of the memory*", as recited in independent claims 8, 11 and 13. Applicant respectfully submits that the suggested combination of references

fails at least because neither reference describes or suggests an arrangement having the ability to "*a logic circuit coupled to the memory array and having a capability to align output data as to a read line of the memory device in accordance with a plurality of different modes*", as recited in independent claims 15 and 20.

The cited reference of Shibata teaches a SDRAM that is always in DLL or PLL mode when operating and has the ability to adjust the DLL to operate stably in various external clock speed ranges. The cited reference of IBM teaches a SGRAM that is always in DLL mode when operating and has a double data read rate and power off mode to reduce power consumption. Applicant respectfully submits that even if the suggested combination of references were to be proper, the combination would still not result in all of the features of the claimed invention, specifically the ability to operate in either a DLL mode, or to operate in a non DLL mode. The claimed invention is capable of operating in either of the two major standard operational modes for DDR SGRAMs, the standard championed by Intel, or the standard championed by IBM. Neither of the two cited references have this claimed feature, and thus no possible motivation could exist for one of ordinary skill in the art to make the suggested combination, nor would the suggested combination result in all of the claimed features of the claimed invention.

The dependent claims are seen as being in patentable condition at least as depending upon independent claims shown above to be patentable over the suggested combination of cited art, and further as containing additional patentable features over the base claims. Dependent claims 3 and 6, for example, recite the feature of "*defaults to the second mode having the non-DLL capability, and enters the first mode having the DLL capability upon receiving a Load Mode Register command on the Extended Mode Register*", which feature can not be suggested by the cited references since neither has a non-DLL operating mode. Applicant respectfully requests that this rejection be reconsidered and withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, David Suhl, at (508) 865-8211 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 16 Nov '04

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 18 day of November, 2004.

Tina Kohut
Name

Signature